MVME300A/D1

MVME300A GPIB Controller with DMA User's Manual

MOTOROLA

MVME300A
GPIB Controller with DMA
User's Manual
(MVME300A/D1)

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PREFACE

This manual provides general information, hardware preparation, installation instructions, and functional description for the MVME300A GPIB Controller with DMA.

This manual is intended for anyone who wants to design OEM systems, supply additional capability to an existing compatible system, or in a lab environment for experimental purposes.

A basic knowledge of computers, and digital logic is assumed.

To use this manual, you should be familiar with the publications listed in the *Related Documentation* paragraph in Chapter 1 of this manual.

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SAFETY SUMMARY
SAFETY DEPENDS ON YOU

The following general safety precautions must be observed during all phases of operation, service, and repair of this equipment. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the equipment. Motorola Inc. assumes no liability for the customer's failure to comply with these requirements. The safety precautions listed below represent warnings of certain dangers of which we are aware. You, as the user of the product, should follow these warnings and all other safety precautions necessary for the safe operation of the equipment in your operating environment.

GROUND THE INSTRUMENT.

To minimize shock hazard, the equipment chassis and enclosure must be connected to an electrical ground. The equipment is supplied with a three-conductor ac power cable. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter, with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE.

Do not operate the equipment in the presence of flammable gases or fumes. Operation of any electrical equipment in such an environment constitutes a definite safety hazard.

KEEP AWAY FROM LIVE CIRCUITS.

Operating personnel must not remove equipment covers. Only Factory Authorized Service Personnel or other qualified maintenance personnel may remove equipment covers for internal subassembly or component replacement or any internal adjustment. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

DO NOT SERVICE OR ADJUST ALONE.

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

USE CAUTION WHEN EXPOSING OR HANDLING THE CRT.

Breakage of the Cathode-Ray Tube (CRT) causes a high-velocity scattering of glass fragments (implosion). To prevent CRT implosion, avoid rough handling or jarring of the equipment. Handling of the CRT should be done only by qualified maintenance personnel using approved safety mask and gloves.

DO NOT SUBSTITUTE PARTS OR MODIFY EQUIPMENT.

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification of the equipment. Contact your local Motorola representative for service and repair to ensure that safety features are maintained.

DANGEROUS PROCEDURE WARNINGS.

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed. You should also employ all other safety precautions which you deem necessary for the operation of the equipment in your operating environment.

WARNING

Dangerous voltages, capable of causing death, are present in this equipment.
Use extreme caution when handling, testing, and adjusting.

(3/91)

CONTENTS

INDEX

FIGURES

TABLES

CHAPTER 1
GENERAL INFORMATION

Introduction

This manual provides general information, preparation for use and installation instructions, operating instructions, and functional description for the MVME300A GPIB Controller with DMA (referred to as the MVME300A throughout this manual).

MVME300A provides you with a complete IEEE-488 bus listener/talker/controller interface for use with a VMEbus system. Several MVME300As may be used as GPIB controllers in a system, each with its own IEEE-488 bus but all controlled by the VMEbus system controller.

NOTE

It is assumed that the reader is thoroughly familiar with the General Purpose Interface Bus (GPIB) as covered in IEEE-488 Specification, 1978 issue as modified in 1980. Refer to the *Related Documentation* section in this chapter.

Features

The features of the MVME300A include:

- VMEbus compatible
- Jumper-selectable VMEbus address modulo 64
- Functions under VMEbus Data Transfer Bus (DTB) slave or master configuration
- DMA for performance enhancement
- 256 bytes or 1Kb of FIFO buffer onboard for DMA latency
- Intelligent VMEbus requester for improved system performance
- Programmable interrupt levels/vectors

- Accessible via a set of 32 onboard registers including 6-bit status register
- Meets complete IEEE-488 1980 standard
- Software-configurable controller, talker, and listener capability (hardware has complete capability, as limited by software)
- Supports up to 300Kb/second data rate on the GPIB interface
- Programmable End-Of-String (EOS) character
- Hardware-selectable GPIB primary address, software-selectable GPIB secondary address
- IEEE-488 connector provided on MVME300A cable
- Onboard LED displays controller FAIL status
- Double-high, single-wide VMEmodule form factor

Specifications

Specifications for the MVME300A are shown in Table 1-1.

Table 1-1. MVME300A Specifications

Characteristics	Specifications
Power requirements	+Vdc ± 5% @ 2.5 A (typical), 3.3 A (maximum)
GPIB Data Transfer Rate	300Kb/sec. maximum
Address lines	A01-A23 as DMA VMEbus master A01-A15 as non-DMA VMEbus slave
Data lines	D00-D07 or D08-D15 as DMA VMEbus master D00-D07 only as non-DMA VMEbus slave
Modes of Operation	Polling, interrupt, and DMA.
Operating temperature	0° to 55° C at point of entry of forced air cooling
Storage temperature	-55° to 85° C
Relative humidity	5% to 90% (non-condensing)
Physical characteristics	(excluding front panel)
Height	9.187 inches (233.35 mm)
Depth	6.299 inches (160.00 mm)
Thickness	0.063 inches (1.6 mm)

General Description

The MVME300A GPIB controller is used to interface the VMEbus with any IEEE-488 standard device(s) for the purpose of transferring data, status, and commands between the device(s) and the VMEbus MPU.

Controller Implemented GPIB Functions

The GPIB functions implemented by MVME300A (using the TMS9914A chip) are as follows:

Interface Function	Capability Code
Source Handshake	SH1
Acceptor Handshake	AH1
Talker, Extended Talker	T5, TE5
Listener, Extended Listener	L3, LE3
Service Request	SR1
Remote Local	RL1
Parallel Poll	PP2, PP1
Device Clear	DC1
Device Trigger	DT1
Controller	C1,2,3,4,9

NOTE

The MVME300A driver available from Motorola does not implement talk only and listen only modes per IEEE-488.

The MVME300A has complete source and acceptor handshake capability. The MVME300A can operate as a basic talker or extended talker and can respond to a serial poll. It may be placed in a talk only mode, and is unaddressed to talk when it receives its untalk command.

The MVME300A can operate as a basic listener or extended listener. It may be placed in a listen only mode, and is unaddressed to listen when it receives its unlisten command.

The MVME300A has full capabilities for requesting service from another controller.

The MVME300A can be placed in local/remote mode.

Full parallel poll capability is included in the MVME300A.

Device clear and device trigger capabilities are also included in the MVME300A.

All controller functions as specified in the IEEE-488-1980 specification are included in the MVME300A.

VMEbus interrupter Module (VBIM) Functions

The MVME300A can have any of three onboard interrupts: from the TMS9914A GPIB control chip, upon the completion of a DMA memory read or write operation, or upon the detection of an error during a DMA memory read or write. These interrupt inputs go to three of the four control registers in the MC68153 VBIM chip. Your software programs these registers to generate any of the seven Interrupt Request (IRQX*) outputs to the VMEbus. Refer to Chapter 4 and the *MC68153 Data Sheet* for details.

NOTE

The unused interrupt control and vector registers may be used as general purpose registers **only** if the DMA capability of the MVME300A is **not** utilized.

Equipment Required

The MVME300A board is connected by cable to an IEEE-488 bus which may have up to 14 other devices connected to it. One or more MVME300A modules are installed in a VMEbus compatible system. The system must contain only one device capable of being the VMEbus system controller. Possible setups are in a VME Microcomputer System or with a MVME110-1 VMEmodule Monoboard Microcomputer.

The MVME300A requires a software driver. Motorola provides such a driver as part of VERSAdos version 4.3 and higher. Refer to the *MVME3SW MVME300A (GPIB Controller with DMA) I/O Driver Reference Manual*. You may, of course, write their own drivers.

Related Documentation

The following publications are applicable to the MVME300A and may provide additional helpful information. If not shipped with this product, they may be purchased from the Motorola, Inc, Technical Literature Center, 1919 West Fairmont Drive, Suite 8, Tempe, AZ 85282; Telephone 1-800-458-6443; FAX (602) 438-0240. Non-Motorola documents may be obtained from the sources listed.

Document Title	Motorola Publication Number
MC68153 Bus Interrupter Module Data Sheet	MC68153
VERSAdos to VME Hardware and Software Configuration User's Manual	MVMEVDOS
MVME300A (GPIB Controller with DMA) I/O Driver Reference Manual	MVME3SW
MVME300A GPIB Controller with DMA Support Information (Refer to the *Support Information* section in this chapter)	SIMVME300A

NOTE: Although not shown in the above list, each Motorola Computer Group manual publication number is suffixed with characters which represent the revision level of the document, such as /D2 (the second revision of a manual); each supplement bears the same number as the manual but has a suffix such as /A1 (the first supplement to the manual).

The following publications are available from the sources indicated.

ANSI/IEEE Std 1014-1987 Versatile Backplane Bus: The Institute of Electrical and Electronics Engineers, Inc., 345 East 47th Street, New York, NY 10017, USA. (VMEbus specification)

IEEE Std. 488-1978 and the Supplement to IEEE Standard Digital Interface for Programmable Instrumentation (IEEE Std. 488A-1980): The Institute of Electrical and Electronics Engineers, Inc., 345 East 47th Street, New York, NY 10017, USA.

TMS9914A General Purpose Interface Bus (GPIB) Controller Data Manual (MP033A): Texas Instruments, Semiconductor Group, P.O. Box 1443, Houston, TX 77001.

Support Information

The SIMVME300A manual contains the connector interconnect signal information, parts list, and the schematics for the MVME300A.

This manual may be obtained free of charge from Motorola, Inc, Technical Literature Center, 1919 West Fairmont Drive, Suite 8, Tempe, AZ 85282; Telephone 1-800-458-6443; FAX (602) 438-0240.

Manual Terminology

Throughout this manual, a convention has been maintained whereby data and address parameters are preceded by a character which specifies the numeric format as follows:

$	dollar	specifies a hexadecimal number
%	percent	specifies a binary number
&	ampersand	specifies a decimal number

Unless otherwise specified, all address references are in hexadecimal throughout this manual.

An asterisk (*) following the signal name for signals which are level significant denotes that the signal is true or valid when the signal is low.

An asterisk (*) following the signal name for signals which are edge significant denotes that the actions initiated by that signal occur on high to low transition.

In this manual, assertion and negation are used to specify forcing a signal to a particular state. In particular, assertion and assert refer to a signal that is active or true; negation and negate indicate a signal that is inactive or false. These terms are used independently of the voltage level (high or low) that they represent.

CHAPTER 2
HARDWARE PREPARATION AND INSTALLATION

Introduction

This chapter provides unpacking instructions, hardware preparation, and installation instructions for the MVME300A.

Unpacking Instructions

NOTE

If the carton is damaged upon receipt, request carrier's agent be present during unpacking/ inspection of equipment.

Unpack equipment from shipping carton. Refer to packing list and verify that all items are present. Save packing material for storing and reshipping of equipment.

Hardware Preparation

To select the desired configuration and ensure proper operation of the MVME300A, certain modifications may be made before installation. These changes are made through jumper arrangements on the headers. The location of the headers, switches, LEDs, and connectors on the MVME300A is illustrated in Figure 2-1. The module has been factory tested and is shipped with factory-installed jumper configurations that are described in the following sections with each header description. The module is operational with factory-installed jumper configurations. The module is configured to provide the system functions required for a VMEbus system. It is necessary to make changes in the jumper arrangements for the following conditions:

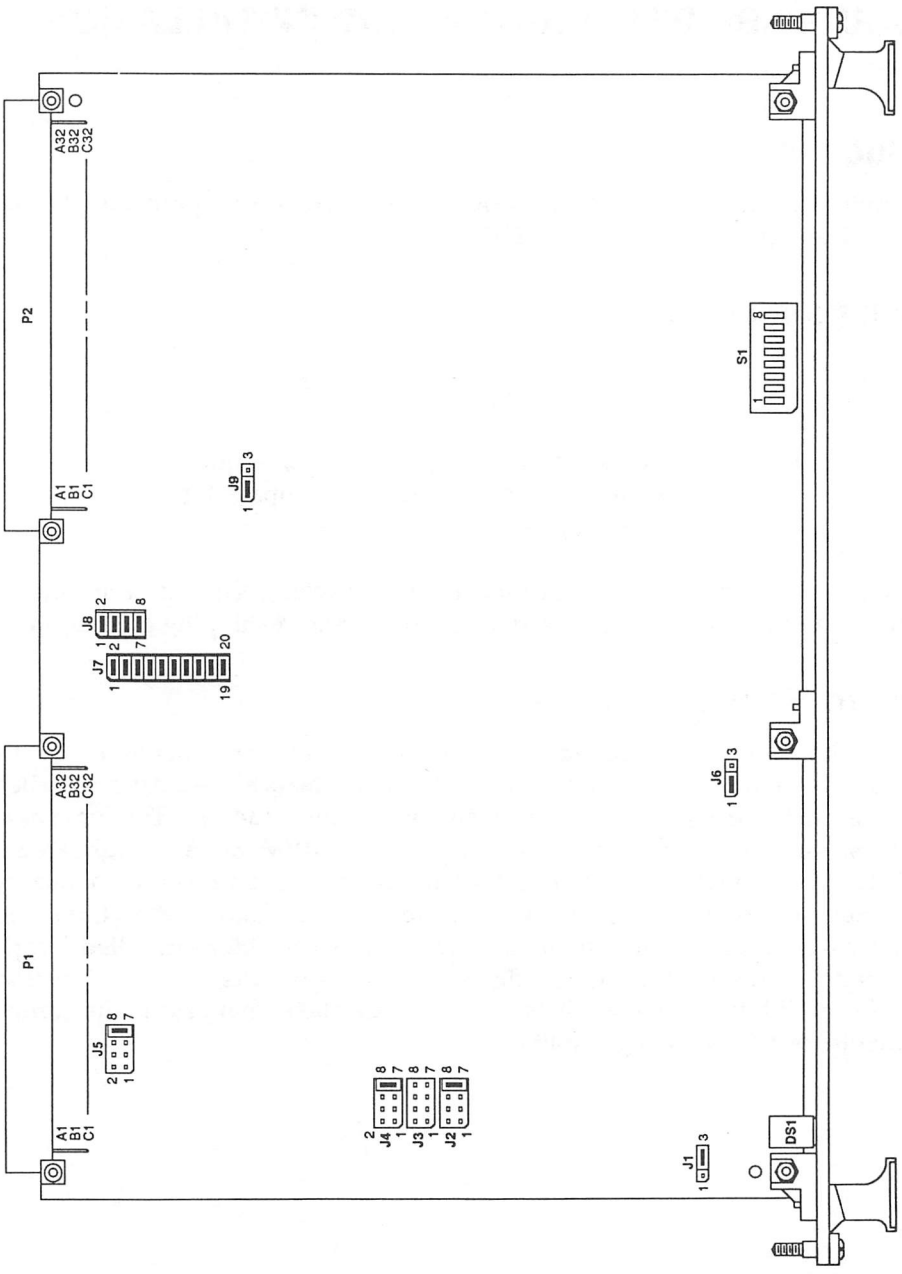


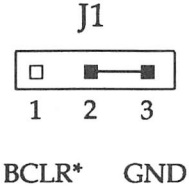
Figure 2-1. MVME300A Header Locations

- BCLR* enable select (J1)
- BGXIN* enable select (J2)
- BGXIN* to BGXOUT* bypass select (J3)
- BGXOUT* enable select (J4)
- BRX* output enable select (J5)
- FIFO RAM controller memory size select (J6)
- VMEbus board base address select (J7)
- VMEbus Release Count Register (VBRCR) count select (J8)
- Three-state or open collector select (J9)

Bus Clear (BCLR*) Enable Select Header (J1)

The figure below shows the factory-installed configuration of header J1 with a jumper between pins 2-3. This simulates a BCLR* active signal, so that the VBRCR control circuits can instruct the VBRCR to finish its count and release the VMEbus to another module. This is necessary if the MVME300A is used with a VMEbus controller such as the MVME110 which has only one level of bus arbitration and cannot drive BCLR* active low.

If the MVME300A module is used with a VMEbus controller which does support all four levels of bus arbitration, then remove the jumper from header J1 pins 2-3, and install a jumper on header J1 between pins 1-2, to connect BCLR* to the VBRCR control circuits on the MVME300A.

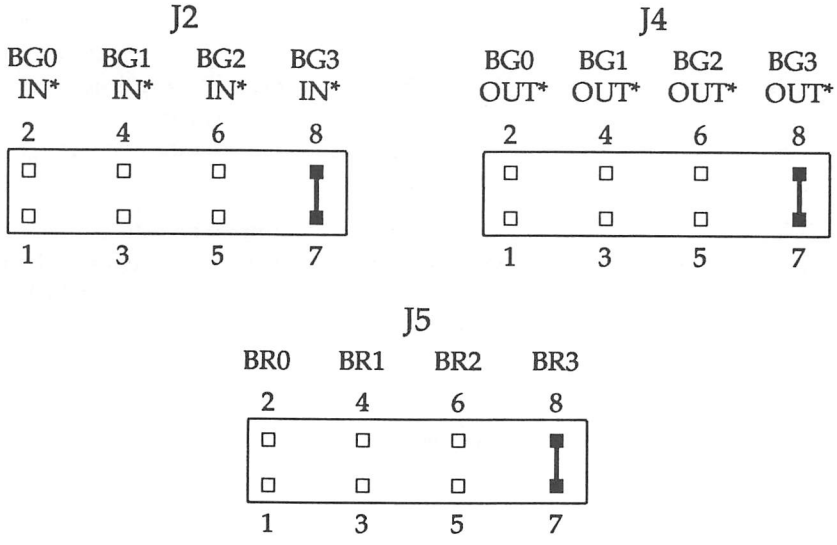


Bus Grant and Bus Request Select Headers (J2,J4,J5)

A MVME300A module can be used with a single level of bus grant and bus request signals by installing one (and only one) jumper in each of the headers J2, J4, and J5. The same level must be used for each header. For example, the figure below shows the factory configuration with one jumper each between pins 7 and 8 of J2, J4, and J5, which enables BG3OUT*, BG3IN*, and BR3*, respectively.

If the MVME300A is used in a system with a VMEbus backplane that has daisy-chain jumpers, find the slot the MVME300A is in. Remove the bus grant jumper on that slot for the single bus grant level selected by J2, J4, and J5. Also remove the Interrupt Acknowledge (IACK) jumper on the same slot, or the interrupter circuits on the MVME300A can not work properly.

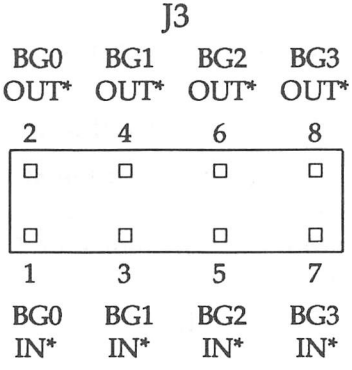
Slot dependence of the MVME300A may be eliminated by installing jumpers on header J3 between pins 1-2, 3-4, 5-6, and 7-8. Remove all jumpers from headers J2,J4, and J5.



BGXIN* to BGXOUT* Bypass Select Header (J3)

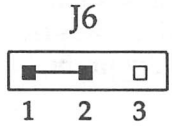
Any jumper installed on header J3 bypasses that particular level of the BGXIN* to BGXOUT* signal daisy-chain around the MVME300A. If the MVME300A is used in a VMEbus system with a backplane that can jumper these bus grant signals, install the jumpers on the backplane for the three bus grant levels not selected by headers J2, J4, and J5. (Refer to the *Bus Grant and Bus Request Select Headers (J2,J4,J5)* section in this chapter.)

If the VMEbus system does not have a backplane with jumpers, or if more than one MVME300A is to be used in the system, install jumpers on header J3 for the three bus grant levels not selected by headers J2, J4 and J5. The figure below shows the factory configuration of J3 with no jumpers installed (no BGXIN* signal bypassed to a BGXOUT* signal).



FIFO RAM Controller Memory Size Select Header (J6)

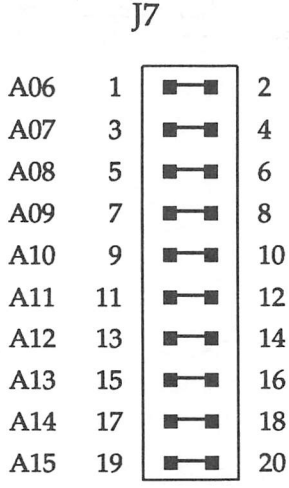
The LS1 and LS2 inputs at pins 12 and 13 of U46, the FIFO RAM controller, select the maximum size of the memory that may be stored in the FIFO RAM U51. As shown in the figure below, the factory-installed configuration is a jumper at header J6 between pins 1-2, which forces LS1 high and selects 256 bytes for the FIFO. If more FIFO storage is needed, remove the jumper from header J6 pins 1-2, and install a jumper at header J6 between pins 2-3, to ground LS1 and select a FIFO size of 1024 bytes (1Kb).



256 Bytes 1024 Bytes

VMEbus Board Base Address Select Header (J7)

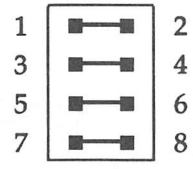
Header J7 is used to select the base address of the MVME300A set of 32 onboard registers modulo 64. The base address is $FFSST0, where 'S' = selected, and low or 0. The figure below shows the factory configuration with all jumpers installed, for a base address of $FF0000.



VMEbus Release Count Register Count Select Header (J8)

Header J8 jumpers set the number of bytes to transfer before the MVME300A releases the VMEbus in DMA mode. The VMEbus Release Count Register (VBRCR) counts the bytes and issues a signal that puts the MVME300A into a VMEbus Data Transfer Bus (DTB) slave configuration. The figure below shows the factory-installed configuration of J8, with all four jumpers installed, giving a count before release of 15 bytes (the maximum possible). Pins 1 and 2 are for the LSB, and pins 7 and 8 are for the MSB.

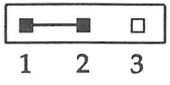
J8



Three-State or Open-Collector Buffer Select Header (J9)

The SN75160A, buffer U65 (for the IEEE-488 data lines) is configured as three-state or open-collector buffers by a jumper at header J9. The factory- installed configuration, as shown in the figure below, is with a jumper across header J9 pins 1-2, which makes U65 open-collector. (PE input is low.) For data transfer rates of 250Kb/second or greater, remove the jumper from header J9 pins 1-2 and install a jumper at header J9 pins 2-3, to configure U65 as three-state.

J9



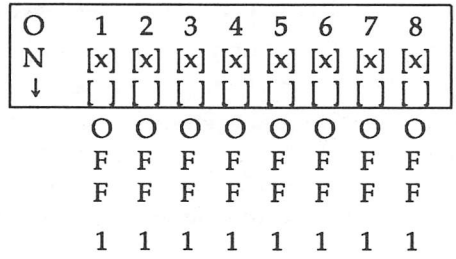
Open-Collector Three-State

GPIB Address Switch (S1)

The 8-segment DIP switch S1, which is accessible from the front panel of the MVME300A, functions as the read portion of the address register (register 20) of the TMS9914A GPIB controller chip U60. The factory-installed configuration is with all switch segments open (see the figure below). Segment 1 open means that the MVME300A is not set up as IEEE-488 system controller. The other pins of S1 can be software configured to mean "don't be a listener" **dal** or "don't be a talker" **dat** flags sent to the software, and a GPIB primary address of 11111 (all five segments 4 through 8 open) = $1F = decimal 31. (The GPIB secondary address is set by software.)

NOTE

The MVME300A driver available from Motorola does not utilize **dal** and **dat**. The address $1F is an illegal IEEE-488 address.



If the system controller segment 1 of S1 is closed, the MVME300A is configured as the IEEE-488 bus system controller.

CAUTION

There can be only one system controller per IEEE-488 bus. More than one system controller makes the bus inoperable and may damage devices on the bus.

Closing the **dal** (disable listener) segment 2 of S1 sends a flag to the software that should be used as a "don't be a listener" function. Closing the **dat** (disable talker) segment 3 of S1 sends a flag to the software that should be used as a "don't be a talker" function.

NOTE

"Talker only" and "listener only" functions are selected by the software for the MVME300A. The MVME300A driver available from Motorola does not implement these functions per IEEE-488.

Closing any of the remaining 5 segments (4 through 8) of S1 puts a 0 on that line of the GPIB primary address, as follows: segment 4 for A4, segment 5 for A3, segment 6 for A2, segment 7 for A1, and/or segment 8 for A0.

Installation Instructions

This section describes how to install the MVME300A in a VMEbus system and how to connect the MVME300A to an IEEE-488 bus. See Figure 2-2.

Installation in a VMEbus System

One or more MVME300A modules may be installed in a system that is VMEbus compatible. Each MVME300A in a system must have a separate VMEbus base address (refer to the *VMEbus Board Base Address Select Header (J5)* section in this chapter). Refer to the *Bus Grant and Bus Request Select Headers (J2, J3, J4)* section in this chapter for backplane bus grant and interrupt acknowledge jumpering. When the MVME300A has been configured as you desire, it can be installed in the system as follows:

1. Turn all equipment power OFF and disconnect power cable from ac power source.

> **CAUTION**
>
> **Connecting modules while power is applied may result in damage to components on the module.**

> **WARNING**
>
> **DANGEROUS VOLTAGES, CAPABLE OF CAUSING DEATH, ARE PRESENT IN THIS EQUIPMENT. USE EXTREME CAUTION WHEN HANDLING, TESTING, AND ADJUSTING.**

2. Remove chassis cover as instructed in the equipment user's manual.
3. Remove the filler panel(s) from the appropriate card slot(s) at the front of the chassis. Do not install in card slot 1 unless the module is configured for system controller (refer to the *GPIB Address Switch (S1)* in this chapter.
4. Insert the MVME300A into the selected card slot. Be sure module is seated properly into the connectors on the backplane. Fasten the module in the chassis with the screws provided.
5. Replace cover (if removed).
6. Turn equipment power ON.

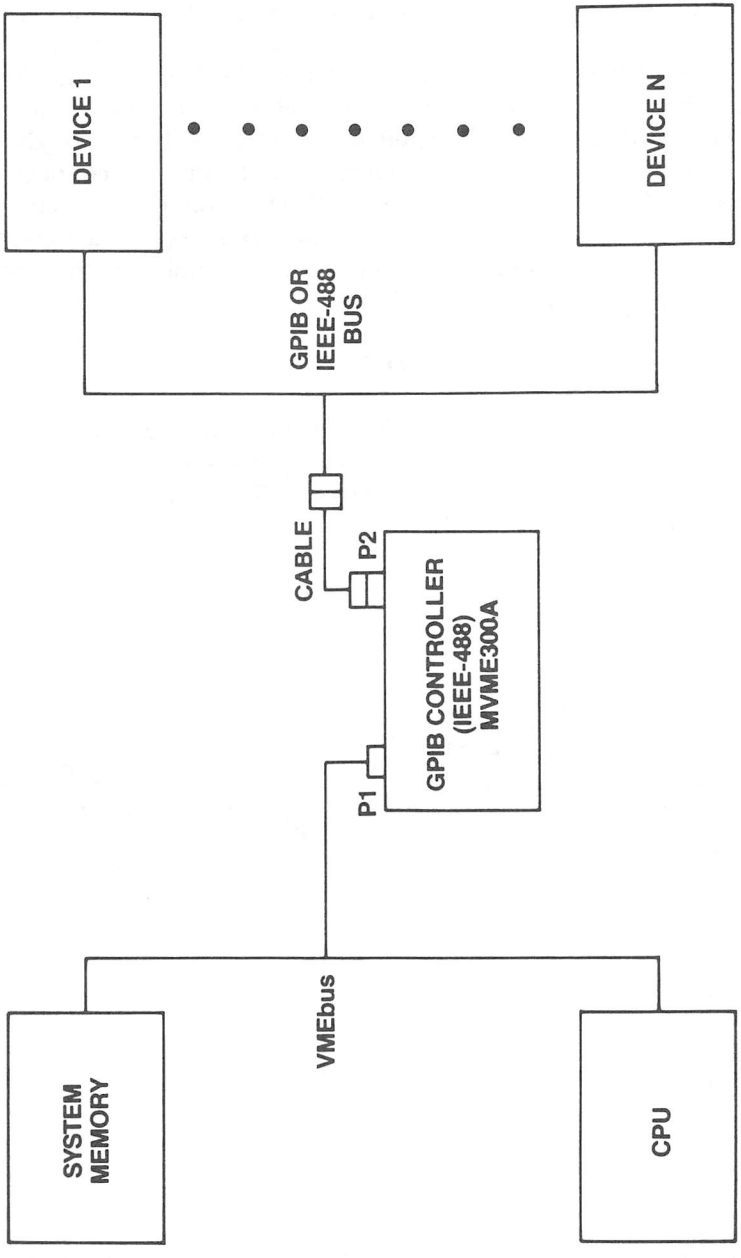


Figure 2-2. MVME300A Installation in a VMEbus System

2

Connection to an IEEE-488 Bus

Each MVME300A module in a system may be connected to a separate IEEE-488 bus, or two or more may be connected to the same bus. If a MVME300A is configured as the GPIB system controller (refer to the *GPIB Address Switch (S1)* section in this chapter), no other device on that bus may be made a system controller. Each MVME300A is connected to an IEEE-488 bus through its cable, which is connected to the DIN 41612 double- row, 64-pin, P2 connector on the MVME300A board. The other end of the MVME300A cable is a standard IEEE-488 24-pin female connector, which must be connected to a 24-pin male connector on the GPIB. If you want to mount the female cable connector on a panel, cut mounting holes in the panel per Figure 2-3.

NOTE

Connector P2 on the MVME300A does not use any of the I/O Channel signals used on many other VMEmodules. Do not connect P2 to an I/O Channel.

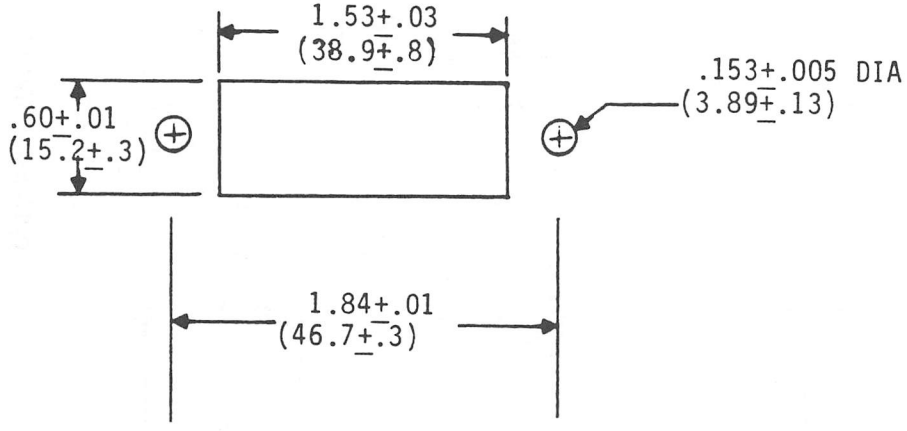


Figure 2-3. Panel Mounting the MVME300A Cable Connector

Software Installation

The MVME300A requires a software driver. Motorola provides such a driver as part of VERSAdos revision 4.3 and higher. The driver must be available to the VMEbus system master. The master can be a MVME110 in a VMEmodule chassis.

CHAPTER 3
OPERATING INSTRUCTIONS

Introduction

This chapter provides the necessary information to initialize and use the MVME300A in a system configuration.

Controls and Indicators

The MVME300A contains one 8-segment DIP switch S1 and one LED FAIL indicator DS1.

GPIB Address Switch

S1 is an 8-segment DIP switch that controls various IEEE-488 bus functions of the MVME300A module. One segment sets up the MVME300A as system controller, the next two segments signal the software to disable the listener or talker functions, and the remaining five segments set up the GPIB primary address for the module. Refer to the *GPIB Address Switch (S1)* section in Chapter 2.

NOTE

The MVME300A driver available from Motorola does not implement talk only and listen only per IEEE-488.

FAIL Indicator

The red LED DS1 is the FAIL indicator. It lights or goes out under the following conditions:

1. DS1 lights when the MVME300A is turned on under VMEbus power up.
2. DS1 lights when the System Reset Signal (SYSRESET*) goes low. This could happen, for example, if the system MPU were a VME110 and the you pressed the RESET button.

3. When a 1 is written to bit 4 of the Uniline Command Register (UCR) on the MVME300A, the STLED onboard signal goes high and sets (lights) DS1. You can write to the UCR via a terminal, or have the software driver do so when desired.
4. When the onboard GCRST signal from the GPIB controller reset register (register number 5) goes high, DS1 goes out. The GCRST signal resets most of the MVME300A hardware, as explained in Chapter 4.

Operating Procedures

No particular initial operating procedures are required by the MVME300A, other than the configuration and installation described in Chapter 2 and the usual steps for powering up the system that the MVME300A is in. Detailed operating procedures depend entirely on the software driver, and must be selected by the customer for the specific instruments on the IEEE-488 bus.

CHAPTER 4
FUNCTIONAL DESCRIPTION

Introduction

This chapter provides a block diagram level description of the MVME300A, including all onboard registers, as well as a description of the DMA read and write modes of operation, VMEbus interrupts, and IEEE-488 bus functions.

Block Diagram Description

A block diagram of MVME300A is shown in Figure 4-3. The MVME300A functions in the slave or master configuration as selected by the host processor. In the DMA mode, the MVME300A functions as master; in the non-DMA mode, the MVME300A functions as a slave device.

The following Data Transfer Bus (DTB) options are exercised when the MVME300A functions as slave:

A16 An A16 slave is capable of decoding 15 address lines (A01-A15). It decodes 15 lines when a short address Address Modifier (AM) code is present on the VMEbus. It does not respond when an extended or standard address code is presented.

D8 A D8 slave is capable of driving and monitoring eight data lines (D0-D7). This allows it to do 8-bit transfers only. Therefore, the MPU should address only the odd byte of the MVME300A registers during read/write operation.

The following DTB options are exercised when the MVME300A is the master:

A24 An A24 master is capable of driving 23 address lines (A01-A23). It drives 23 lines with a valid address whenever it places a standard address AM code on the bus. It is never allowed to place an extended address code on the bus.

When master, the MVME300A addresses both the odd and even bytes of the memory location. Therefore, the data in the memory must be sequentially organized in even and odd bytes.

D8 A D8 master is capable of driving and monitoring 16 data lines, although it drives or monitors only eight lines at any time. This allows it to do 8-bit transfers on either (D0-D7) or (D8-D15).

The MVME300A uses 64 contiguous memory locations (bytes) in the upper 64Kb of the memory map ($FF0000 and up). The host processor can access the MVME300A via a set of 32 onboard read/write registers. Each register is located at a consecutive odd and even address of the memory. However, the host processor should address the odd byte to read or write to a register.

The VME address bus (A1-A15) is decoded to select one of the 32 registers, using an 8-bit comparator U48 (74LS682) and two decoders, U40 and U12 (74S138 and 74S139). An address modifier register U21 is provided for the MPU to load the register with the appropriate code before MVME300A becomes the master.

When the MVME300A functions in the DMA mode, the data is transferred to and from the devices via the onboard FIFO U51 by a common Internal Data Bus (IDBSX). The FIFO consists of 256/1Kb of buffer and is controlled by RAM FIFO controller U46.

NOTE

Whenever the MVME300A is commanded to perform DMA transfers, none of its registers should be accessed from the VMEbus until the MVME300A signals DMA completion (or DMA aborted) by generating an interrupt on the VMEbus.

A 6-bit status register is provided onboard that can be read by enabling the three-state drivers U57.

The TMS9914A GPIB controller U60 is used to interface between the IEEE-488-1980 GPIB and the MPU/DMA Controller. Communication with the microprocessor is done via 13 read/write registers of the TMS9914A.

Discrete logic is used to implement the DMA control of the MVME300A. The DMA control logic consists of a 24-bit Memory Address Register (MAR) (U24, U25, U30, U31, U36, U37), a 16-bit Byte Count Register (BCR) (U19, U20, U41, U42), VBRCR (U82), and a UCR (U14).

The VMEbus interrupter module U47 is used as the interrupter requester on the GPIB controller.

The rest of the control circuits of the MVME300A are implemented synchronously using discrete logic.

An 8-position DIP switch S1 is provided for device address selection, disable talk/listen functions and system controller selection.

MVME300A Registers

The MVME300A appears to the CPU as a set of 64 contiguous memory locations (bytes), or registers, in the overall memory map. The host processor accesses the MVME300A via a set of 32 onboard read/write registers. Each register is located at a consecutive odd and even address in the memory. However, the host processor should address the odd byte to read or write to a register. The VMEbus address bits (A1-A5) are decoded to select one of the 32 registers.

The rest of the address bits (A6-A15) are jumper selectable. Therefore, the MVME300A registers can appear contiguously anywhere in the upper 64K of the memory map by properly selecting the base address. Table 4-1 lists the MVME300A registers and their addresses.

NOTE

All the registers, except the VBRCR and MARX, are cleared either by the RESET GPIBC command or by the SYSRESET* signal on the VMEbus.

Table 4-1. MVME300A Registers

Reg No.	Function	Data Bus Bits (Note 1)	Type	VMEbus Address Lines					Address Offset (Hex)
				A5	A4	A3	A2	A1	
	Register Bank 1								
0	Mem Addr Reg 1	D7-D0	R/W	0	0	0	0	0	1
1	Mem Addr Reg 2	D7-D0	R/W	0	0	0	0	1	3
2	Mem Addr Reg 3	D7-D0	R/W	0	0	0	1	0	5
3	Byte Cnt Reg 1	D7-D0	W	0	0	0	1	1	7
4	Byte Cnt Reg 2	D7-D0	W	0	0	1	0	0	9
5	Reset GPIBC	X	W	0	0	1	0	1	B
6	Addr Mod Reg	D5-D0	R/W	0	0	1	1	0	D
7	Stat Reg	D5-D0	R	0	0	1	1	1	F

Table 4-1. MVME300A Registers (cont'd)

Reg No.	Function	Data Bus Bits (Note 1)	Type	VMEbus Address Lines A5	A4	A3	A2	A1	Address Offset (Hex)
	Register Bank 2								
8	VMEbus Rel Cnt Reg	X	W	0	1	0	0	0	11
9	EOS Char Cmp Reg	D7-D0	W	0	1	0	0	1	13
10	Uniline Command Reg	D5-D0	W	0	1	0	1	0	15
11	FIFO Data I/O Reg	D7-D0	R/W	0	1	0	1	1	17
12	Not used			0	1	1	0	0	19
13	Not used			0	1	1	0	1	1B
14	Not used			0	1	1	1	0	1D
15	Not used			0	1	1	1	1	1F
	Register Bank 3: (Note 2)	**TMS9914A Registers**							
	Read Reg	**Write Reg**							
16	Int Stat 0	Int Mask 0		1	0	0	0	0	21
17	Int Stat 1	Int Mask 1		1	0	0	0	1	23
18	Addr Stat	Not used		1	0	0	1	0	25
19	Bus Stat	Aux Cmd		1	0	0	1	1	27
20	Addr SW1 (Note 3)	Addr Reg		1	0	1	0	0	29
21	Not used	Serial Poll		1	0	1	0	1	2B
22	Cmd Pass Thru	Parallel Poll		1	0	1	1	0	2D
23	Data In	Data Out		1	0	1	1	1	2F

Table 4-1. MVME300A Registers (cont'd)

Reg No.	Function	Data Bus Bits (Note 1)	Type	VMEbus Address Lines A5	A4	A3	A2	A1	Address Offset (Hex)
	Register Bank 4: (Note 4)	**Interrupter Registers**							
24	Cont Reg 0		R/W	1	1	0	0	0	31
25	Cont Reg 1		R/W	1	1	0	0	1	33
26	Cont REg 2		R/W	1	1	0	1	0	35
27	Cont Reg 3		R/W	1	1	0	1	1	37
28	Vector Reg 0		R/W	1	1	1	0	0	39
29	Vector Reg 1		R/W	1	1	1	0	1	3B
30	Vector Reg 2		R/W	1	1	1	1	0	3D
31	Vector Reg 3		R/W	1	1	1	1	1	3F

NOTES: 1. X = Don't care data.
2. Refer to the Texas Instruments TMS9914A GPIB Controller Data Manual.
3. The switch SW1 on the MVME300A module functions as the read register corresponding to the address register on the TMS9914A chip.
4. Refer to the Motorola MC68153 Bus Interrupter Module Data Sheet.

Memory Address Registers MAR1, MAR2, MAR3

The MAR consists of three 8-bit registers (U36 and U37, U30 and U31, U24 and U25) to form a 24-bit address register. The least significant bit IA00 of this register is used to generate the upper or lower data strobes (MIDS0 and MIDS1). Before a DMA data transfer, the MAR is loaded by software with the starting memory address. This register is updated by the MVME300A hardware between each byte transfer.

MAR1 contains the least significant 8-bits of the address bus (A7-A0). MAR2 contains address bits A15-A8, and MAR3 contains address bits A23-A16. All three registers are readable and writable by the CPU.

Byte Count Registers BCR1, BCR2

The byte count register consists of two 8-bit registers (U41 and U42, U19 and U20) to form a 16-bit byte count register. Before a DMA data transfer, this register is loaded by the software with the 1's complement of the number of bytes to be transferred. The register is used when the MVME300A is the talker and when it is the listener. This register provides you with the capability of transferring up to 64Kb of data over the GPIB in any one given DMA operation. The contents of this register are automatically incremented between byte transfers and the VMEbus.

BCR1 contains the least significant eight bits of the count, and BCR2 contains the most significant eight bits of the byte count.

These two registers are writable only by the MPU.

The carry from this register is latched as a GPIBC status bit, Byte Count Register Done (BCRDN). (Refer to the *Controller Status Register (CSREG)* section in this chapter.

GPIB Controller Reset Register (GCRST)

Writing to this register through U66 (data is don't care) would generate the GCRST signal to reset all the hardware on the controller board except the VBRCR and MAR. This command is ORed with the VMEbus signal SYSRESET*. However, a software command must be issued to the TMS9914A auxiliary command register to reset those functions that are not resettable by the hardware reset.

Address Modifier Register (AMR)

This register, U21 and U15, consists of six bits (D5 through D0). The register is loaded by the software prior to the DMA operation. When the MVME300A becomes master, the contents of this register are used to assert the address modifier lines of the VMEbus, while accessing the system memory on the VMEbus.

This register is readable and writable by the CPU.

Controller Status Register (CSREG)

A 6-bit (S5-S0) status register, U57, is provided onboard. This is a read only register. It is to be noted that this register holds the status of the onboard activities and is not part of the TMS9914A status register. The contents of this register are not cleared at the completion of read status cycle.

Each bit of this status register represents a status as explained in Table 4-2.

Table 4-2. Controller Status Register (CSREG) Bits

Bit	Status Description
S0	FIFO empty
S1	EODNE: This status indicates that when the controller is in the listen mode, either an end-of-string (EOS) character has been received or the EOI signal has been detected and that the FIFO is empty. This bit is cleared by either a reset controller command (GCRST) or SYSRESET* or by writing $20 (hexadecimal) to the UCR.
S2	FIFO FULL
S3	BCRDN: Byte Count Register Done. This bit indicates that the byte count register has counted up during DMARD/DMAWRT operation. This bit is cleared by writing $20 (hexadecimal) to the UCR.
S4	SYSFAIL: This bit indicates that the front panel system FAIL LED on the controller module has been set. The LED is set during power on and also by writing $10 (hexadecimal) to the UCR. This bit can be cleared by the reset controller command.
S5	BERR: Bus Error. This bit is set during DMARD/DMAWRT when the memory board responds with a BERR* signal due to an invalid memory access. This bit is cleared by master reset or writing $20 (hexadecimal) to the UCR.

VMEbus Release Count Register (VBRCR)

This register, U82, is composed of four bits, and is a write only register. This register is used only when the MVME300A functions in the DMA mode. The purpose of this register is as follows. The MVME300A holds the VMEbus during DMA read/write operation until a high priority device bus request comes through, at which point the MVME300A releases the bus only after transferring the number

of bytes as specified in the VBRCR. Jumpers at header J8 are provided to load this register with the 1's complement of any number from 0 to 15. The software must load the register prior to a DMA operation.

End-of-String (EOS) Character Compare Register (ESCCR)

In most of the GPIB systems, it is desirable to terminate an incoming data transmission with an EOS character. This requires the ability to compare each data byte with the given terminating character. The TMS9914A lacks this ability. Therefore, external logic is added to detect EOS. However, this logic has to be enabled by the software (refer to the *Uniline Command Register (UCR)* section in this chapter.

The ESCCR, U52, is part of the EOS detect logic and is an 8-bit write only register. This register must be loaded with the character to be compared. The EOS detect logic, U55, compares the 8-bit byte previously written to the compare register. When a compare is found, that condition is latched and used in generating DMA operation (listener) complete interrupt when the FIFO becomes empty. The logic of the 8-bit byte to be loaded to this register is determined to be positive.

Uniline Command Register (UCR)

This 6-bit (D5-D0) write only register (U14, U95D, and U6C) is a multipurpose register used to receive GPIB controller commands from the CPU. The bit assignments and their functions are explained in Table 4-3.

Table 4-3. Uniline Command Register (UCR) Bits

Bit	Name	Description
D0=1;	DMA Write	
D1=1;	Enable EOS character compare	This command is issued to enable the EOS detect logic on the MVME300A module. The EOS character compare register must be loaded with the character that is to be compared with the incoming character. Writing a 1 to this bit enables the EOS detect logic.
D2=1;	DMA READ	Talker function
D3=1;	Not used	
D4=1;	Set SYSFAIL LED	Writing this bit to the register sets the front panel system FAIL LED on the module.
D5=1;	Clear BCRDN, FIFO, and BERR	Byte Count Register Done (BCRDN) bit, FIFO Controller U46, and Bus Error (BERR) bit are cleared by writing 1 to the UCR. D0 and D2 must be low.

NOTE Writing to this register by the software must be done as the last step during DMA initialization, because the MVME300A logic starts to function as soon as the register is set with DMA WRITE or DMA READ bit. Once the DMA command is issued (via this register), none of the MVME300A registers should be accessed until the board signals DMA completion (or DMA aborted) by generating an interrupt on the VMEbus.

FIFO Data I/O Register (FDIOR)

This data I/O register, U51, is an 8-bit read/write register. This is not a TMS9914A Data I/O register.

This register is used primarily in the DMA mode; however, it may be used by the CPU to write and read data for diagnostic purposes. During normal operation, this register is used only when the MVME300A functions as master in the DMA read/write. After the MVME300A becomes master and during DMA write operation, the contents of this register are activated on the lower data bus byte (D0-D7) or the upper data bus byte (D8-D15), depending on the lower or upper data strobes. During DMA read operation, the FIFO data I/O register would be loaded with the lower data bus byte or the upper data bus byte.

An onboard FIFO controller U46 controls the shift in, shift out logic of the FIFO and is completely transparent to your software.

TMS9914A Registers

Texas Instruments TMS9914A GPIB adapter U60 is used to interface the IEEE-488 GPIB and the host system. Refer to the *TMS9914A Data Manual* for a detailed description of the architecture and software requirements. (Refer to the *Related Documentation* section in Chapter 1.

To access the TMS9914A registers at the completion of a DMA transfer, write $20 to the Uniline Command Register (UCR). The contents of the Controller Status Register (CSREG) is cleared at the completion of this operation. Refer to the *Controller Status Register (CSREG)* section in this chapter.

VMEbus Interrupter Module (VBIM) Registers

The VBIM, U47, is used as an interrupt requester on the MVME300A. A detailed description of this module can be found in the bus interrupter module data sheet. (Refer to the *Related Documentation* section in Chapter 1.

The features of this module are summarized as follows:

- LSI support of VMEbus
- Handles four sources of interrupts
- Eight programmable read/write registers for interrupt control and interrupt vector storage
- Programmable vectors
- Programmable interrupt levels
- 40-pin DIP
- Uses TTL-compatible macrocell array and replaces up to 40 TTL ICs

Data Transfer Under DMA Mode

The basic function of the MVME300A is to implement the GPIB functions as specified by IEEE-488 standards. These functions can be divided into two groups.

Group 1 consists of functions such as talker, listener, and controller, which are implemented using the TMS9914A along with the DMA logic onboard the MVME300A. A major part of the MVME300A hardware logic is used to implement talker and listener functions in the DMA mode.

Group 2 consists of functions such as remote local, service request, parallel poll, device trigger, and device clear. These functions are also implemented using the TMS9914A. However, the implementation of these functions does not require any major onboard hardware logic; instead, it requires carefully thought-out software algorithms.

From the above discussion, it is evident that one of the main design objectives of the MVME300A is to transfer data (talker/listener) under DMA mode, between GPIB and system memory, which implies that the MVME300A is using the VMEbus throughout the DMA operation. However, this poses system performance degradation problems when other devices on the VMEbus need the bus during the MVME300A DMA operation.

Therefore, considerations of other devices on the VMEbus have been taken such that the MVME300A releases the VMEbus whenever a higher/lower priority device requests the usage of the VMEbus. This philosophy is implemented by providing 256 (or 1024) bytes of FIFO on the MVME300A and designing the bus requester circuits of the module in such a way as to release and request the bus, so that, the controller circuits of the MVME300A module can do DMA without slowing down the data rate, and can share the systems most important resource, the VMEbus, with other devices effectively.

DMA Read Operation (Talker Function)

The controller module can be addressed to talk either locally by the host processor, or remotely by the controller-in-charge (see Figure 4-2 for a read operation flow chart.

In the local mode, the TMS9914A enters into Talker Active State (TACS) when the host MPU issues the auxiliary commands **ton** (talk only) followed by **gts** (go to standby) to TMS9914A. Your software may initialize the DMA control before issuing the auxiliary commands to the TMS9914A. Initialization of DMA control involves setting up MAR, BCR, UCR, address modifier register, etc.

In the remote mode, when the controller-in-charge addresses the talker, the TMS9914A enters talker addressed state and generates My Address (MA) interrupt with Accept Data State (ACDS) hold off. Your software may initialize the DMA control before releasing the ACDS hold off, at which time the TMS9914A enters into talker active state.

The controller module then requests the VMEbus. When the grant is issued, the controller module starts reading bytes of data from memory and shifts into the FIFO. When the first byte is available at the output of FIFO, the central control of MVME300A loads that byte into the data out register of the TMS9914A. This

process continues until the last byte is read from the memory (BCRDN is set). During this DMA operation, a bus request could come through from other devices on the VMEbus. The bus request may be from a higher priority device, or a lower or equal priority device.

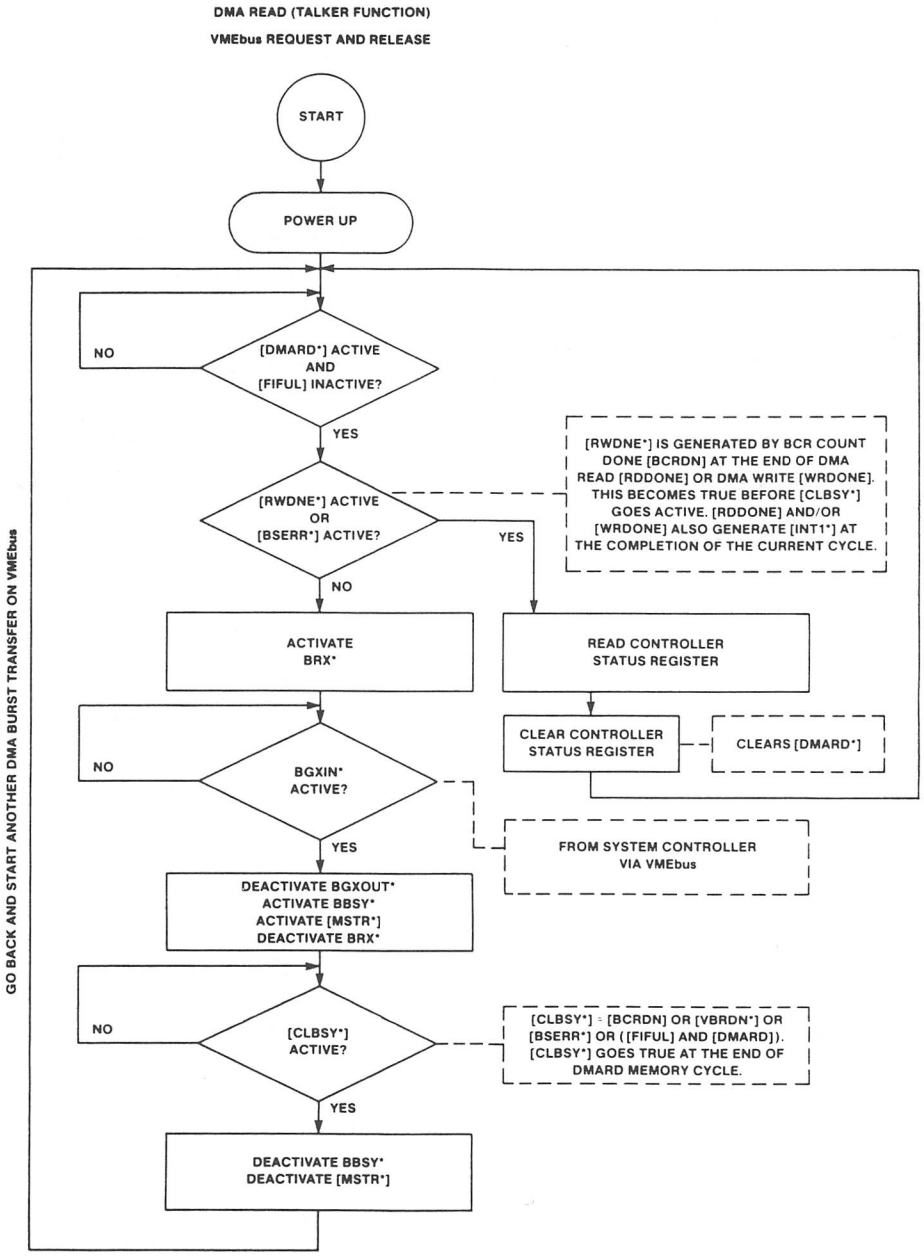


Figure 4-1. Read Operation Flow Chart (Sheet 1 of 3)

DMA READ (TALKER FUNCTION)

DATA TRANSFER FROM SYSTEM MEMORY TO VME300 FIFO

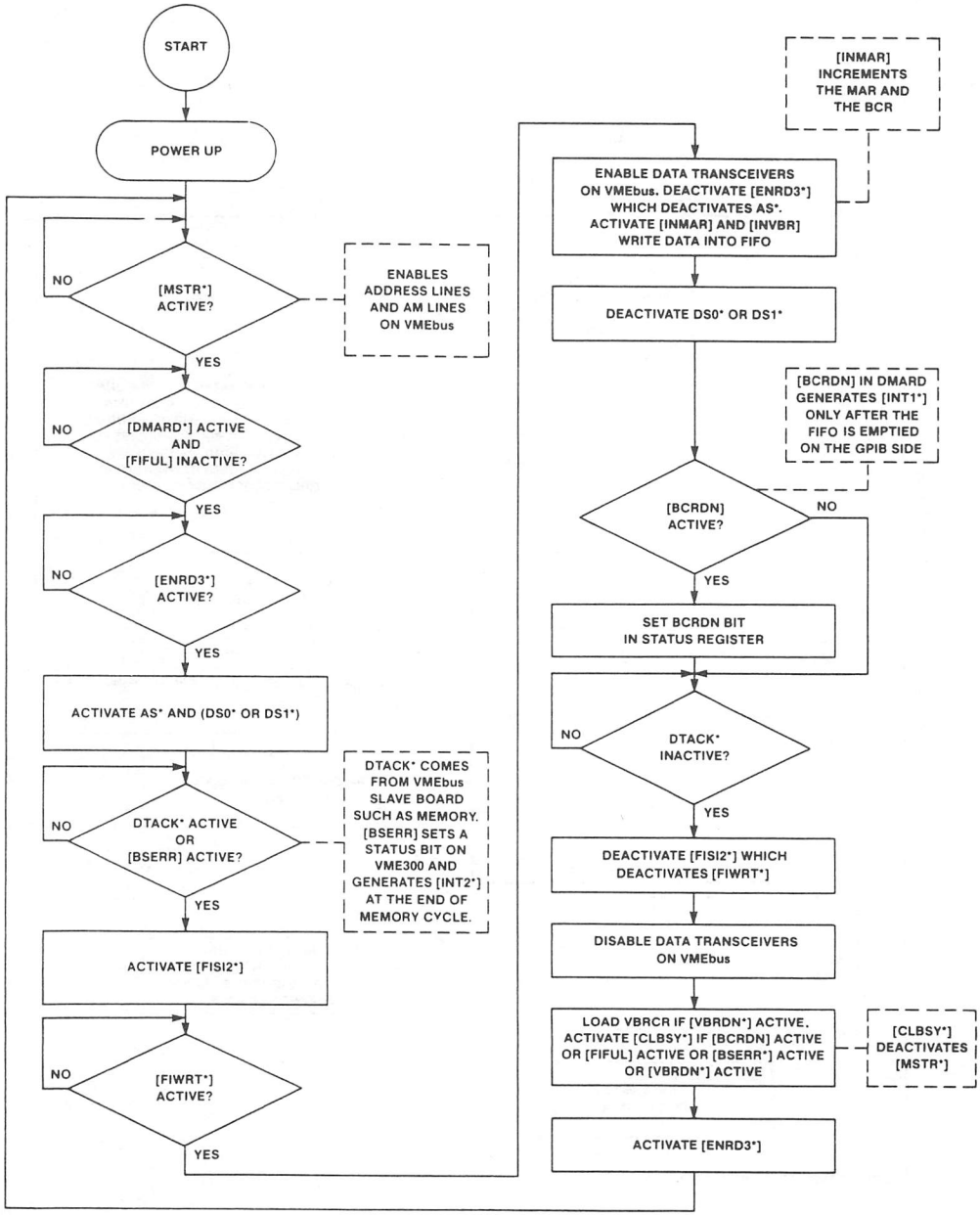


Figure 4-1. Read Operation Flow Chart (Sheet 2 of 3)

Figure 4-1. Read Operation Flow Chart (Sheet 3 of 3)

When the bus request is from a higher priority device (indicated by the VMEbus signal BCLR*), the MVME300A bus requester logic releases the bus only after transferring the number of bytes specified in the VMEbus release count register or when the DMA is done, whichever happens first. When the bus request is from a lower or an equal priority device, then the bus requester releases the bus only when the DMA is complete.

After releasing the bus, if the DMA is still pending, the bus requester requests the bus immediately following the release of the bus. The VMEbus release count register is loaded by the MVME300A at the same time.

If you want to transfer n bytes and send an EOI with the last byte, first transfer n-1 bytes under DMA. An end-of-operation interrupt is generated at the end of the n-1 bytes of DMA. You should then issue the **send-EOI-with-next-byte** command to the TMS9914A auxiliary command register, and then write the nth byte to the data-out register of the TMS9914A. If you do not want to send an EOI, send the n bytes under DMA.

DMA Write Operation (Listener Function)

The controller module can be addressed to listen either locally by the host processor, or remotely by the controller in charge (see Figure 4-3 for a write operation flow chart.

In the local mode, the TMS9914A enters into Listener Active State (LACS) when the host CPU issues the auxiliary commands **lon** (listen only) followed by **gts** (go to stand by) to TMS9914A. Your software may initialize the DMA control before issuing the auxiliary command to TMS9914A.

In the remote mode, when the controller-in-charge addresses the listener, the TMS9914A enters into Listener Addressed State (LADS) and generates My Address (MA) interrupt with Accept Data State (ACDS) hold off. Your software may initialize the DMA control before releasing the ACDS hold off, at which time the TMS9914A enters into Listener Active State (LACS).

The MVME300A then starts reading bytes of data from the **data in** register of the TMS9914A and shifts into the FIFO. When the first byte is available at the output of FIFO, the MVME300A requests the VMEbus. When the grant is issued, the central control of the MVME300A starts to write data bytes from FIFO into the memory. This process continues until the last byte is written into the memory which is indicated either by EOI set, or by EOS detected, or by BCRDN.

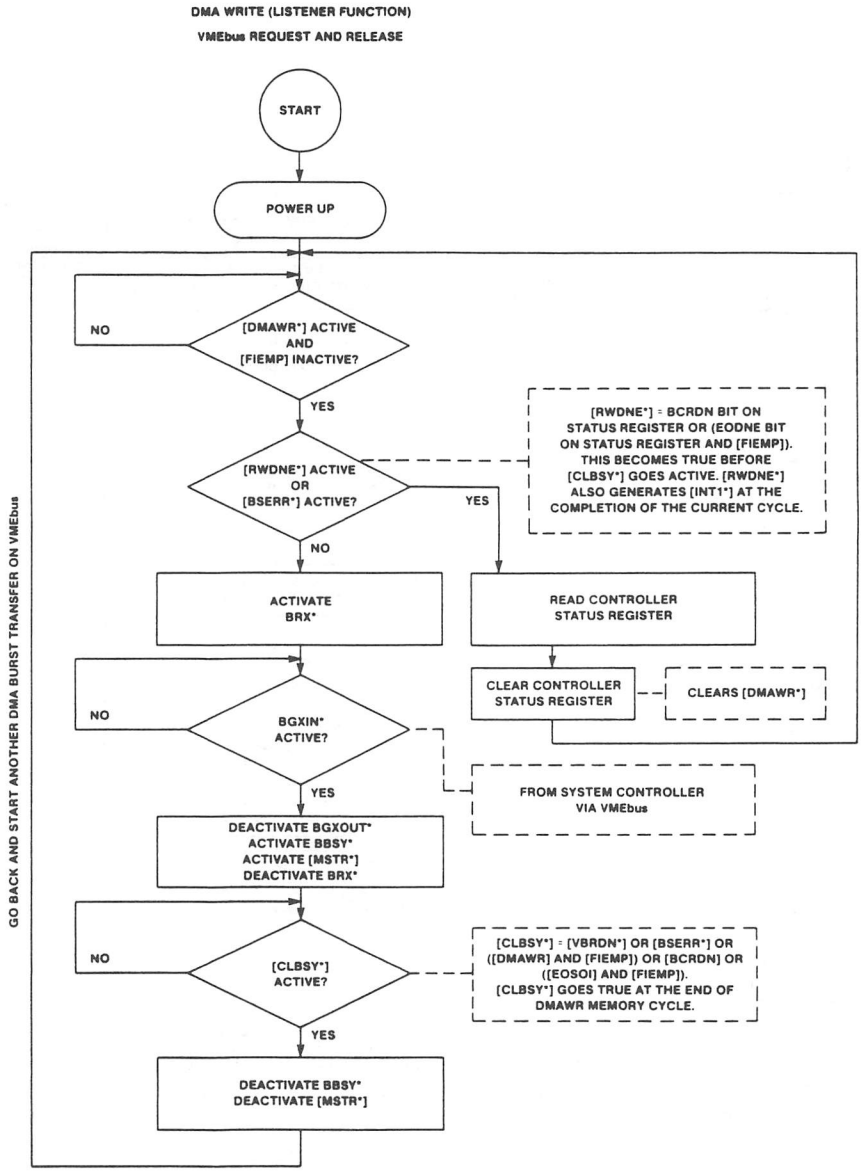


Figure 4-2. Write Operation Flow Chart (Sheet 1 of 3)

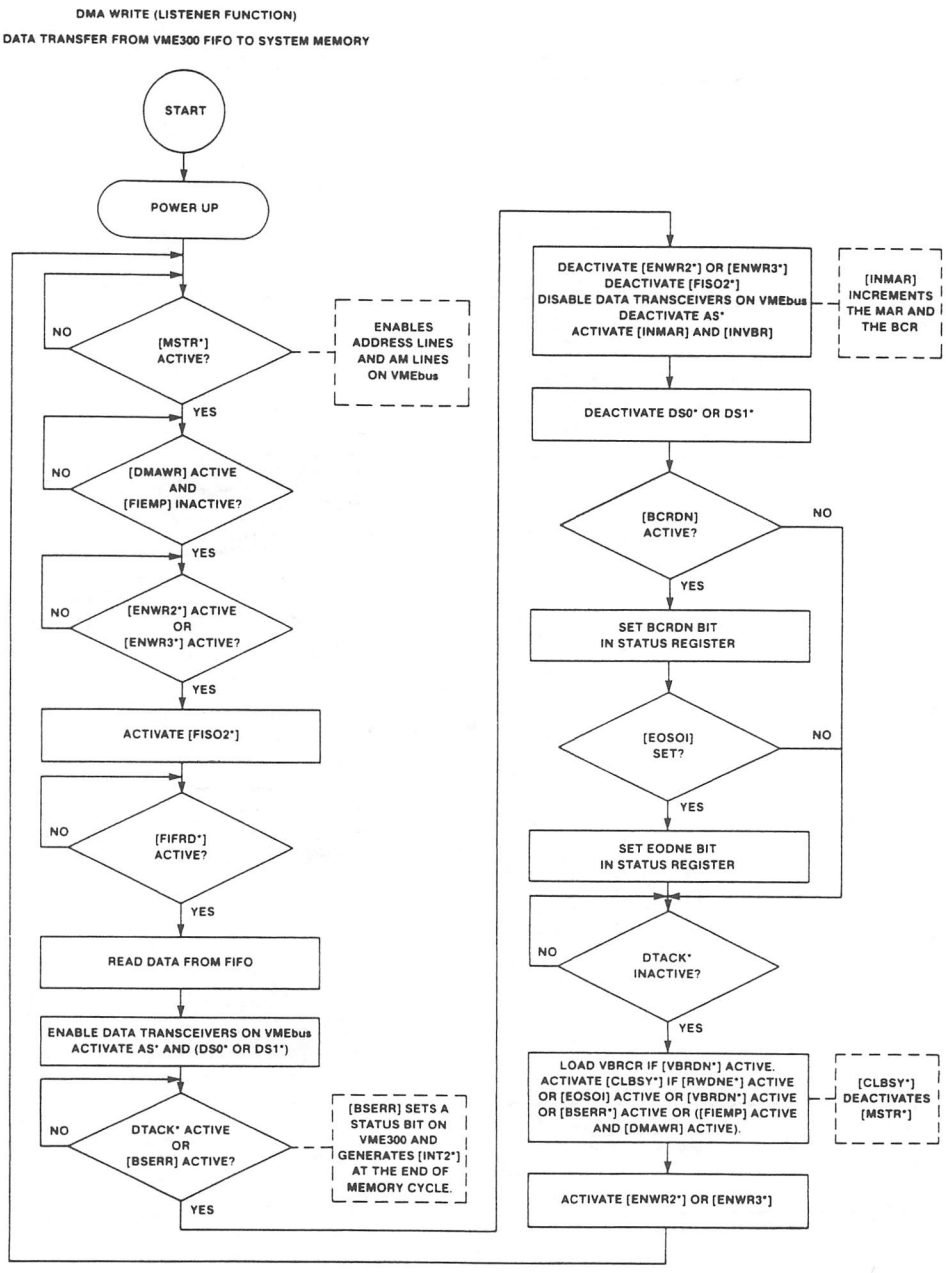


Figure 4-2. Write Operation Flow Chart (Sheet 2 of 3)

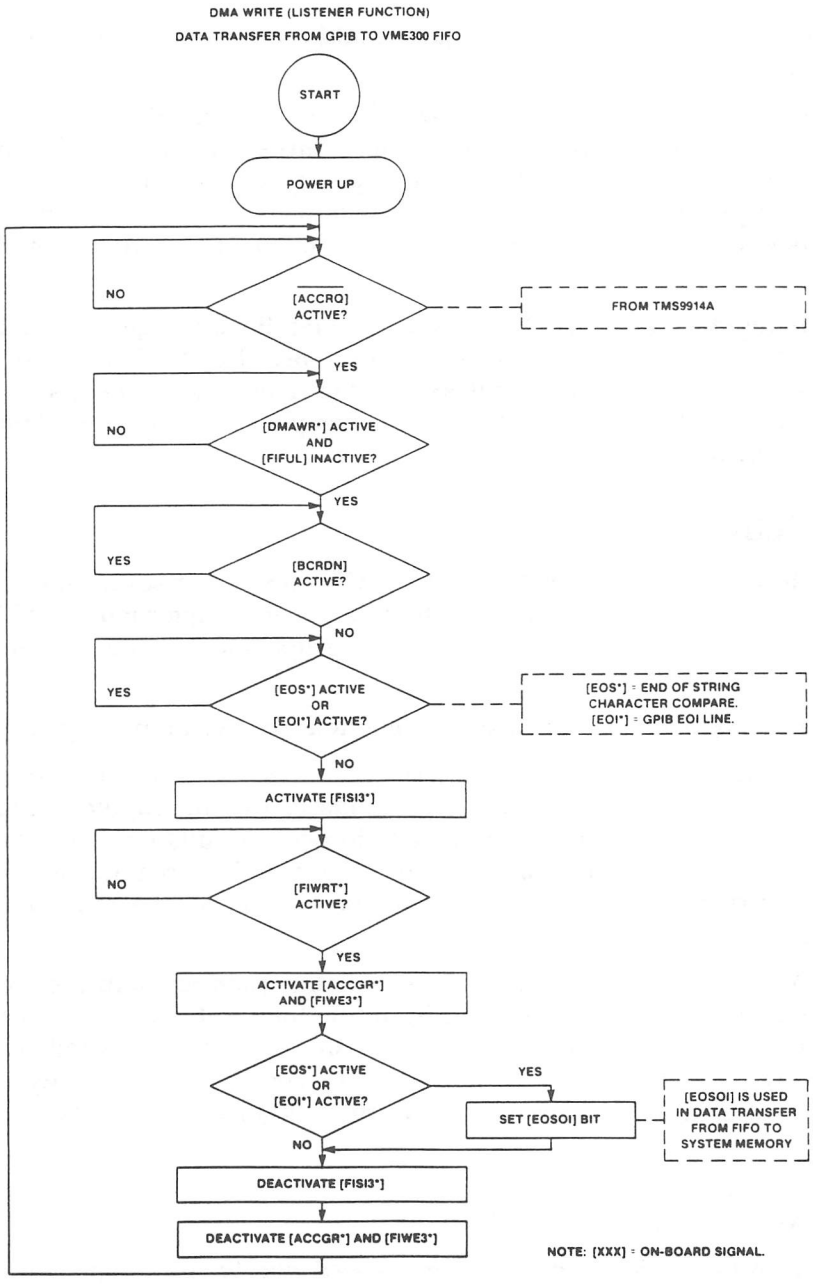


Figure 4-2. Write Operation Flow Chart (Sheet 3 of 3)

During this DMA operation, a bus request could come through from other devices on the VMEbus.

When the bus request is from a higher priority device, the MVME300A bus requester logic releases the bus only after transferring the number of bytes specified in the VMEbus release count register or when the DMA is done, whichever happens first. When the bus request is from a lower or an equal priority device, the bus requester releases the bus only when the DMA is complete.

After releasing the bus, if the DMA is still pending, the bus requester requests the bus immediately following the release of the bus. The VMEbus release count register is also loaded by the MVME300A at the same time. An end-of-operation interrupt is generated by MVME300A at the completion of the entire DMA write (listener) operation.

MVME300A Interrupts

The MVME300A can interrupt the VMEbus CPU on one of seven interrupt lines (IRQ1*-IRQ7*). The MVME300A uses the VMEbus interrupter module U47 as the interrupt requester. The selection of the interrupt line is done via the control register of the interrupter module.

The interrupter module is capable of handling four sources of interrupts.

There are three direct interrupt sources on the MVME300A that are directly connected to three of the four interrupt inputs of the interrupter module. The software can program the interrupt module to generate IRQ on any of the seven interrupt lines on the VMEbus. Your software can also program to have three different interrupt vectors, one for each interrupt source, or have the same vector for each of the interrupt sources.

TMS9914A INT into INT0 on the U47 VBIM is the interrupt from the TMS9914A and is the logical NOR of INT0 and INT1 in the Interrupt Status 0 register of the TMS9914A when masked on. INT0 and INT1 are set only on the condition that at least one event occurs in status registers 0 and 1 and the corresponding bit in the interrupt mask register is also set; i.e., INT0 = (BI(S) and BI(M)) or (BO(S) and (BO(M)).

BI(S) is the interrupt status bit BI
BI(M) is the interrupt mask bit BI

INT1* into INT1 on U47 is the interrupt caused due to the completion of DMA operation (read/write).

INT2* into INT2 on U47 is the interrupt generated by MVME300A due to an error in the memory read/write cycle under DMA mode. This error is caused by the BERR* signal from the slave on the VMEbus.

The INT3 input of U47 is wired high.

MVME300A Implemented GPIB Functions

The GPIB functions implemented by the MVME300A are listed as follows:

Interface Function	Capability Code
Source Handshake	SH1
Acceptor Handshake	AH1
Talker, Extended Talker	T5, TE5
Listener, Extended Listener	L3, LE3
Service Request	SR1
Remote Local	RL1
Parallel Poll	PP2, PP1
Device Clear	DC1
Device Trigger	DT1
Controller	C1,2,3,4,9

NOTE

The MVME300A driver available from Motorola does not implement talk only and listen only modes per IEEE-488.

The MVME300A has complete source and acceptor handshake capability. The MVME300A can operate as a basic talker or extended talker and can respond to a serial poll. It may be placed in a talk only mode, and is unaddressed to talk when it receives its untalk command.

The MVME300A can operate as a basic listener or extended listener. It may be placed in a listen only mode, and is unaddressed to listen when it receives its unlisten command.

The MVME300A has full capabilities for requesting service from another controller.

The ability to place the MVME300A in local/remote mode is included.

Full parallel poll capability is included in the MVME300A.

Device clear and device trigger capabilities are also included in the MVME300A.

All controller functions as specified in the IEEE-488-1980 specification are included in the MVME300A.

Talker Function

The MVME300A implements both the standard talker (T) and extended talker (TE) functions. A detailed flow diagram explaining the sequence of events that take place during talker operation is shown in Figure 4-2.

The MVME300A can be programmed to talk either in the DMA mode or non-DMA mode.

There are four logical operating modes for the talker function. These modes are implemented as follows:

Talker mode 1: Talker mode 1 inhibits both the talker and extended talker functions; i.e., no talker ability. This mode is implemented by the setting the **dat** bit in the address register of TMS9914A. This would disable talk functions. (This is done by a segment of switch S1.)

Talker mode 2: Talker mode 2 implements the standard talker capability. This mode is implemented by not setting the **dat** bit in the address register of TMS9914A. The MVME300A goes to Talker Addressed State (TADS) after it is addressed to talk.

Talker mode 3: In this mode the MVME300A must receive its primary talker address and a secondary talker address. This mode is implemented by controlling the APT mask bit in the TMS9914A interrupt mask register 1. If secondary addressing is required the APT mask bit is set to one during initialization. Refer to secondary addressing in the TMS9914A data manual.

Talker mode 4: Talker mode 4 implements a talk only function. This mode is implemented by issuing a "ton" command to the TMS9914A. The "ton" is included for use in systems without controller. However, where the TMS9914A is being used as a controller, it utilizes the **ton** functions to set itself up as a talker. Care must be taken, therefore, to ensure this function is reset if sending Other Talk Address (OTA).

Listener Function

The MVME300A implements both the standard listener (L) and extended listener (LE) functions. A detailed flow diagram explaining the sequence of events that take place during listener operation is shown in Figure 4-3.

The MVME300A can be programmed to listen either in DMA mode or non-DMA mode.

There are four logical operating modes for the listener function. These modes are implemented as follows:

Listener mode 1: Listener mode 1 inhibits both the listener and extended listener functions; i.e., no listener ability. This mode is implemented by setting the **dal** bit in the address register of the TMS9914A. This would disable listen functions. (This is done by a segment of switch S1.)

Listener mode 2: Listener mode 2 implements the standard listener capability. This mode is implemented by not setting **dal** bit in the TMS9914A address register. The MVME300A goes to the Listener Addressed State (LADS) after it is addressed to listen.

Listener mode 3: In this mode, the MVME300A must receive its primary listener address and a secondary listener address. This mode is implemented by controlling the APT mask bit in the TMS9914A interrupt mask register 1. If secondary addressing is required, the APT mask is set to one during initialization. Refer to the *Secondary Addressing* section in the *TMS9914A Data Manual*.

Listener mode 4: Listener mode 4 implements a listen only function. This mode is implemented by issuing a **lon** command to the TMS9914A. The **lon** is included for use in systems without controller. However, where the TMS9914A is being used as a controller, it utilizes the "lon" functions to set itself up as a listener. Care must be taken, therefore, to ensure this function is reset if sending unlisten (UNL).

Controller Function

NOTE

The MVME300A driver available from Motorola does not implement all controller functions per IEEE-488.

All controller functions as specified by the IEEE-488 Standards are included in the MVME300A. These include the capability to:

1. Be system controller
2. Send remote enable
3. Initialize the interface
4. Respond to service request
5. Send multi-line command messages
6. Receive control
7. Pass control
8. Conduct a parallel poll
9. Conduct a serial poll
10. Take control synchronously or asynchronously

Refer to address switch register for system controller option. (This is done by a segment of switch S1.)

INDEX

When using this index, keep in mind that a page number indicates only where referenced material begins; it may extend to the following page or pages.

F

G

H

I

L

M

N

O

P

R

S

T

U

V

W

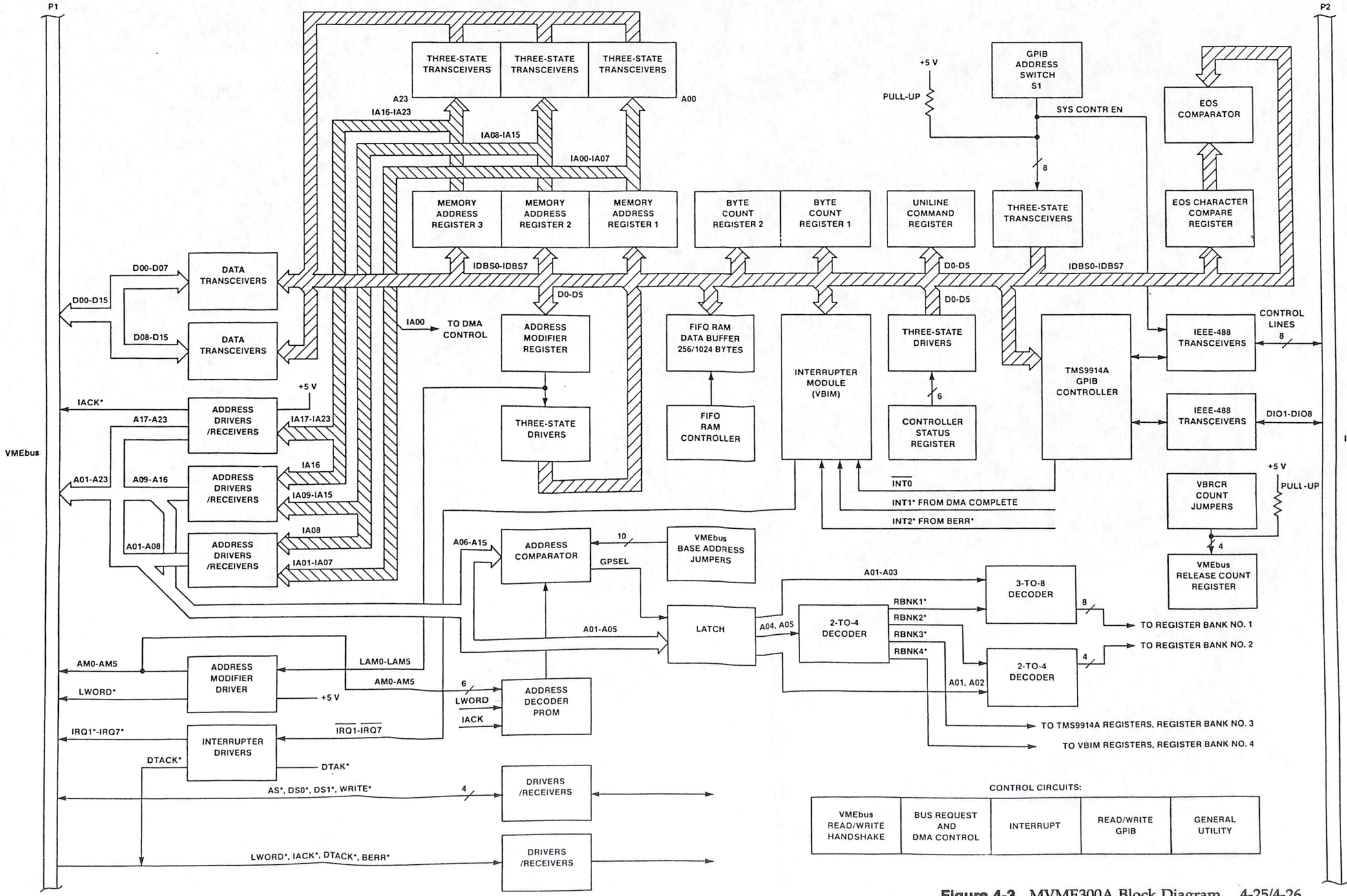


Figure 4-3. MVME300A Block Diagram 4-25/4-26

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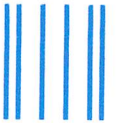

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